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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/211,718	12/14/1998	ERIC R. FOSSUM	08305/015001	9540

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EXAMINER	
GENCO, BRIAN C	

ART UNIT	PAPER NUMBER
2615	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/211,718	FOSSUM ET AL.	
	Examiner	Art Unit	
	Brian C Genco	2615	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 March 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-13 and 17-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-13 and 17-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Applicant's arguments filed March 2, 2005 have been fully considered but they are not persuasive.

Applicant's amendments and arguments with regards to claim 21 have overcome the rejection under 35 USC 112.

Applicant arguments stem from an incorrect interpretation of the Schick reference. It is Applicant's opinion that the Schick reference is that the description on column 5, lines 15-20 teaches to move the inactive area 202 of Fig. 2A away from the edge of the chip to allow room for the substrate bonding area 203. Examiner respectfully disagrees with this interpretation of the reference.

In particular, Examiner notes that the description on column 5, lines 15-20 is in reference to Fig. 1b. In order to understand the context of this section one must look at the entire description from column 4, line 57 – column 5, line 35 wherein it is described that it is desirable that the active area of the sensors are sufficiently close to one another. As such, the aim of this passage is to minimize the space between two adjacent arrays of pixels, i.e., the space between the arrays of pixels 106 and the array of pixels 107 of Fig. 1b. Schick goes on to disclose that ordinary CMOS active pixel devices have a column of drive transistors along one edge of the device which can increase the width of the inactive region at the sensor's boundary on column 5, lines 15-18. It is clear that this column of drive transistors on an ordinary CMOS active pixel device is in fact the row logic of the pixel device such as that illustrated in Fig. 1c. One of ordinary skill in the art would clearly recognize that this is indeed what Schick meant since

Schick discloses that it would increase the inactive region at the sensor's boundary, i.e., the inactive region between the arrays of pixels 106 and the array of pixels 107 of Fig. 1b. So as to provide further clarity, Examiner notes that Schick is in no way referencing the inactive regions 103 since these regions do not occur along any of the borders between the pixel arrays. Schick goes on to disclose that it is advantageous to move the column of drive transistors away from the edge of the device so as to divide the inactive region into two narrower inactive regions, i.e., moving the row logic illustrated in Fig. 1c away from the edge. Examiner notes that Schick teaches this divides the inactive region, i.e., the region caused by the space between each sensor and the row logic, into two narrower inactive regions, i.e., a narrow inactive region from the row logic which has been moved away from the edge and a narrow inactive region from the space between the two sensors.

Examiner notes that in the rejection Fig. 2A was merely relied upon as a clear reference from which to align the claim limitations wherein one skilled in the art would clearly recognize that the image sensor illustrated in Fig. 2A has been rotated by 90° compared to the image sensors 106 and 107 of Fig. 1b discussed above.

As such, Applicants arguments against the rejections on pages 9-12 of the response are not deemed persuasive in view of the above correct interpretation of the Schick reference.

Applicant points out on page 11 of the response that the Office Action on the bottom of page 3 appears to end abruptly. Examiner notes that this is due to a typographical error by the Examiner in copying the exact claim language instead of ending page 3 with a period.

Further, on page 11 of the response Applicant argues that an explanation of the rejection of claim 8 was not found. Examiner notes that claim 8 was not rejected by Schick in view of Heller but was rejected on pages 7 and 8 of the Office Action by Schick in view of Spivey.

Applicant's arguments that the citation of additional references in dependent claims causes the citation of the independent claim to be improper is not deemed persuasive. For example, on page 13 of the response Applicant argues that since claim 5 depends from claim 1 and Spivey was additionally used to reject claim 5 but was not used to reject claim 1, then the citation of references used in the rejection of claim 1 is somehow incorrect. Examiner notes that it would have been improper to have additionally cited Spivey in the rejection of claim 1 since Spivey was not used in the rejection of claim 1. It is unclear what Applicant desires in making these arguments. Examiner respectfully requests Applicant to further explain what they mean.

Applicant argues on page 14 of the response that in order to combine Schick with Sayag there would need to be motivation for placing an inactive area in the center of Schick's active area, wherein there is no motivation to do so.

In response, Examiner notes that there is explicit motivation in Schick on column 5, line 15-20 to do just that.

Applicant argues that Schick teaches away from providing a central inactive area.

In response, Examiner respectfully disagrees. It is Examiner's position that is precisely what Schick teaches to do. Furthermore, in order for Schick to teach away from providing a

central inactive area there would have to be explicit teaching of not providing a central inactive area. Should Applicant continue with this argument, Applicant is requested to indicate a column and line number where Schick teaches that it is disadvantageous or that it is not desired to provide a central inactive area.

Applicant argues that Schick and Spivey teach directly away from including an inactive area centrally in the image sensor.

Examiner respectfully disagrees and requests that Applicant particularly point out the column and line numbers of where Schick and Spivey teach directly away from including an inactive area centrally in the image sensor.

Claim Rejections - 35 USC § 103

The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

Claims 1-4, 9-11, 13 and 17-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over (USPN 5,834,782 to Schick et al.) in view of (USPN 6,396,539 to Heller et al.).

In regards to claim 1 Schick discloses a CMOS image sensor circuit, comprising:

a CMOS image sensor chip comprising an image sensor portion comprising an array of pixels arranged in rows and columns, and a control portion comprising image sensor logic, said image sensor logic being electrically connected to said image sensor portion (e.g., Figs. 2a and 2b; column 4, lines 46-56), said image sensor logic including row logic associated with each of said rows individually, and chip logic associated with parts of said image sensor portion other

than rows individually, said image sensor portion having a first area and a second area (e.g., column 5, lines 15-20 wherein the first area is on one side of the column drive transistors which have been moved away from the edge, and the second area is on the other side of the column drive transistors),

said chip being formed to have at least a first set of parallel edges including a first edge and a second edge, and a second set of parallel edges, different than said first set of parallel edges, said second set of parallel edges including a third edge and a fourth edge (e.g., Figs. 1a, 1b, 2a, and 2b, wherein as shown in Fig. 2a the first edge is on the top, the second edge is on the bottom, the third edge is on the left, and the fourth edge is on the right),

said image sensor portion including imaging pixels extending between said first edge, said second edge, and said third edge, such that imaging pixels of said first area of said image sensor portion are adjacent said first edge and said third edge of said chip and imaging pixels of said second area of said image sensor portion are adjacent said second edge and said third edge of said chip (e.g., Figs. 1a, 1b, 2a, 2b; column 5, lines 15-20),

said row logic being physically located inside said image sensor portion in place of a plurality of pixels of the array forming said image sensor portion (e.g., column 5, lines 15-20); and

It is also known in the art to use on-chip pixel interpolation as taught by Heller et al, herein Heller. Heller discloses having an on-chip memory and controller unit for storing defective pixel locations so that the controller can interpolate values for the defective pixels from the surrounding pixels (e.g., column 8, lines 39-65; column 4, lines 5-9). Note that Heller discloses that it is preferable to include as much circuitry on-chip in order to reduce cost (column

1, line 56 – column 2, line 36). Therefore it would have been obvious to one of ordinary skill in the art at the time of the invention to have preformed pixel interpolation on-chip in order to reduce cost. Furthermore it would have been obvious to one of ordinary skill in the art at the time of the invention to have place the pixel interpolator between said image area and said fourth edge so as to maintain the chip structure disclosed by Schick to still enable butting for the creation of a large format array, namely placing the pixel interpolator in the non-active region 202 of Fig. 2A.

In regards to claim 2 Examiner notes that Schick does not explicitly disclose that the row logic is formed in place of two columns of the array, however, it is clear from Schick's disclosure that the row logic would take the place of the number of columns that the row logic was wide, i.e., if the row logic was two pixels wide then it would take the place of two columns. Examiner notes that it is well known in the art to provide row logic that is two pixels wide or less in order to minimize the amount of dead space on the image sensor. Official Notice is taken. As such, one of ordinary skill in the art would have provided row logic that is two pixels wide or less in order to minimize the amount of dead space on the image sensor.

In regards to claim 3 see Fig. 1b and column 4, line 57 – column 5, line 14.

In regards to claim 4, see Fig. 1a.

In regards to claim 9 see Examiners notes on the rejection of claim 1. Examiner notes that the term centralized is being interpreted to mean anywhere not on an edge.

In regards to claim 10 see Figs. 1b, 1c, 3, 4a.

In regards to claim 11 see Examiners notes on the rejection of claim 1. Note column 5, lines 21-35 wherein the outputs of each image sensor are combined. Further note that the

claimed limitation of integrating the control portions of said at least two CMOS image sensors in inherent with providing a large format image sensor as disclosed by Schick. Examiner notes that the term centralized is being interpreted to mean anywhere not on an edge.

In regards to claim 13 see Examiners notes on the rejection of claim 1. Note the disclosure of abutting image sensor together in Fig. 1b so as to form a large format array.

In regards to claim 17 see Examiners notes on the rejection of claim 1. Examiner notes that the term centralized is being interpreted to mean anywhere not on an edge.

In regards to claim 18 see Examiners notes on the rejection of claims 1 and 11

In regards to claim 19 see Examiners notes on the rejection of claim 2.

In regards to claim 20 note that Schick discloses the row logic is inactive in column 5, lines 15-20.

In regards to claim 21 see Examiners notes on the rejection of claim 1. Examiner notes that it is extremely well known for row logic in CMOS image sensors to have row drivers and row memory in order to decode a row selection input. Official notice is taken. Therefore it would have been obvious to one skilled in the art at the time of the invention to have utilized row drivers and row memory in order to decode a row selection input of Schick's CMOS image sensor.

In regards to claim 22 see Examiners notes on the rejection of claim 1. See also Figs. 1b, and 1c. Note that image sensors 11 and 12 of Fig. 3, sensors 11 and 21 of Fig. 4A.

Claims 5 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over (USPN 5,834,782 to Schick et al.) in view of (USPN 6,396,539 to Heller et al.) in further view of (USPN 5,886,353 to Spivey et al.).

In regards to claims 5 and 12 see Examiners notes on the rejection of claims 1 and 11. Schick nor Heller disclose nor preclude interpolating missing pixels on said chip caused by both said row select logic and by spaces between pixel pitches along abutted edges of said image sensor chips. It is know to do this as taught by Spivey on column 15, lines 30-37 in order to reduce the effect of dead spots. Therefore it would have been obvious to one of ordinary skill in the art at the time of the invention to have interpolated missing pixels caused by both said row select logic and by spaces between said image sensor chips in order to reduce the effect of dead spots.

Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over (USPN 5,834,782 to Schick et al.) in view of (USPN 6,396,539 to Heller et al.) in view of (USPN 5,510,623 to Sayag).

In regards to claim 6 Examiner notes that while Schick discloses that the row logic is moved away from the edge, there is no disclosure that it is necessarily in the center of the plurality of pixels. Sayag discloses the known structure of providing the row logic in the center of the plurality of pixels as shown in Fig. 1. Therefore it would have been obvious to one skilled in the art at the time of the invention to have provided the row logic in the center as suggested by Schick and explicitly disclosed by Sayag in order to provide a symmetric image sensor.

Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over (USPN 5,834,782 to Schick et al.) in view of (USPN 6,396,539 to Heller et al.) in view of (US PG PUB 20020000549 to Spartiotis et al.).

In regards to claim 7, neither Schick nor Heller disclose the usage of a guard ring. Spartiotis discloses to use a guard ring element 40 in paragraph 0047 in order to reduce edge non-uniformities in the region of the edge-most contacts. Therefore it would have been obvious to one of ordinary skill in the art at the time of the invention to have added a guard ring to Schick's image sensors in order to reduce edge non-uniformities in the region of the edge-most contacts.

Claim 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over (USPN 5,834,782 to Schick et al.) in view of (USPN 5,886,353 to Spivey et al.).

In regards to claim 8 Schick discloses a method of capturing an image, comprising:

providing at leas two image sensor chips, each chip having first and second parallel edges and an image sensor array of imaging pixels that comes within two pixel pitches of said first and second edges, and includes a control portion with row selecting logic in place of a plurality of central pixels of the image sensor array between said first and second edges (e.g., column 5, lines 4-20; Fig. 1b);

abutting said image sensor chips along at least one of corresponding first and second edges (e.g., Figs. 1B, 1C, 3, and 4A-4C).

Schick does not disclose nor preclude interpolating missing pixels on said chip caused by both said row select logic and by spaces between pixel pitches along abutted edges of said image

sensor chips. It is know to do this as taught by Spivey on column 15, lines 30-37 in order to reduce the effect of dead spots. Therefore it would have been obvious to one of ordinary skill in the art at the time of the invention to have interpolated missing pixels caused by both said row select logic and by spaces between said image sensor chips in order to reduce the effect of dead spots.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Brian C. Genco who can be reached by phone at 571-272-7364 or by fax at 571-273-7364. The examiner can normally be reached on Monday thru Friday 8:30am to 4:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, James Groody can be reached at 571-272-7950. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the customer service office whose telephone number is 571-272-2600.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Brian C Genco
Examiner
Art Unit 2615

April 14, 2005

TUAN HO
PRIMARY EXAMINER